Electromigration in Integrated Circuits

Workshop on Reliability and Physical Verification, IIT Delhi, 12 Dec 2009

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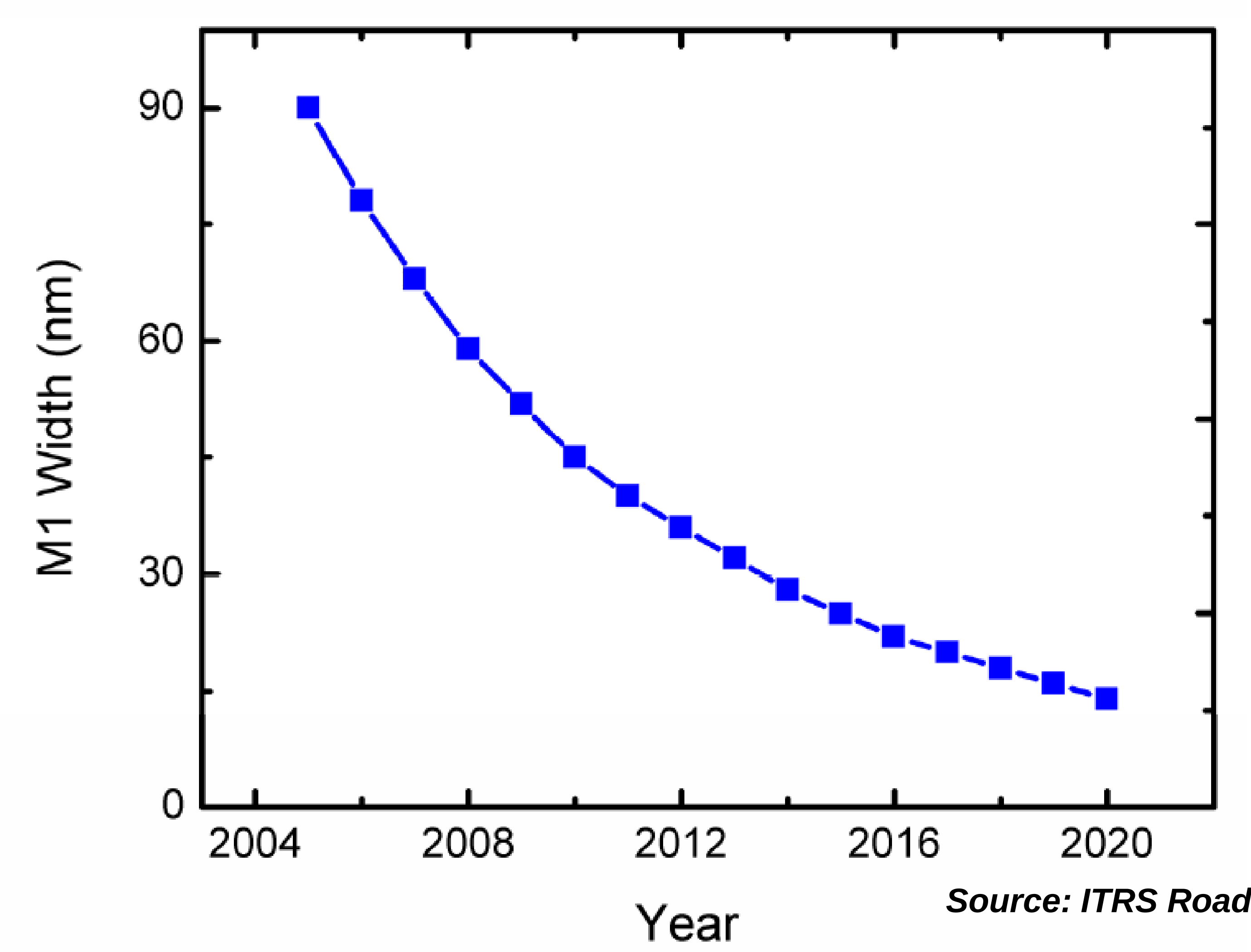
Agenda

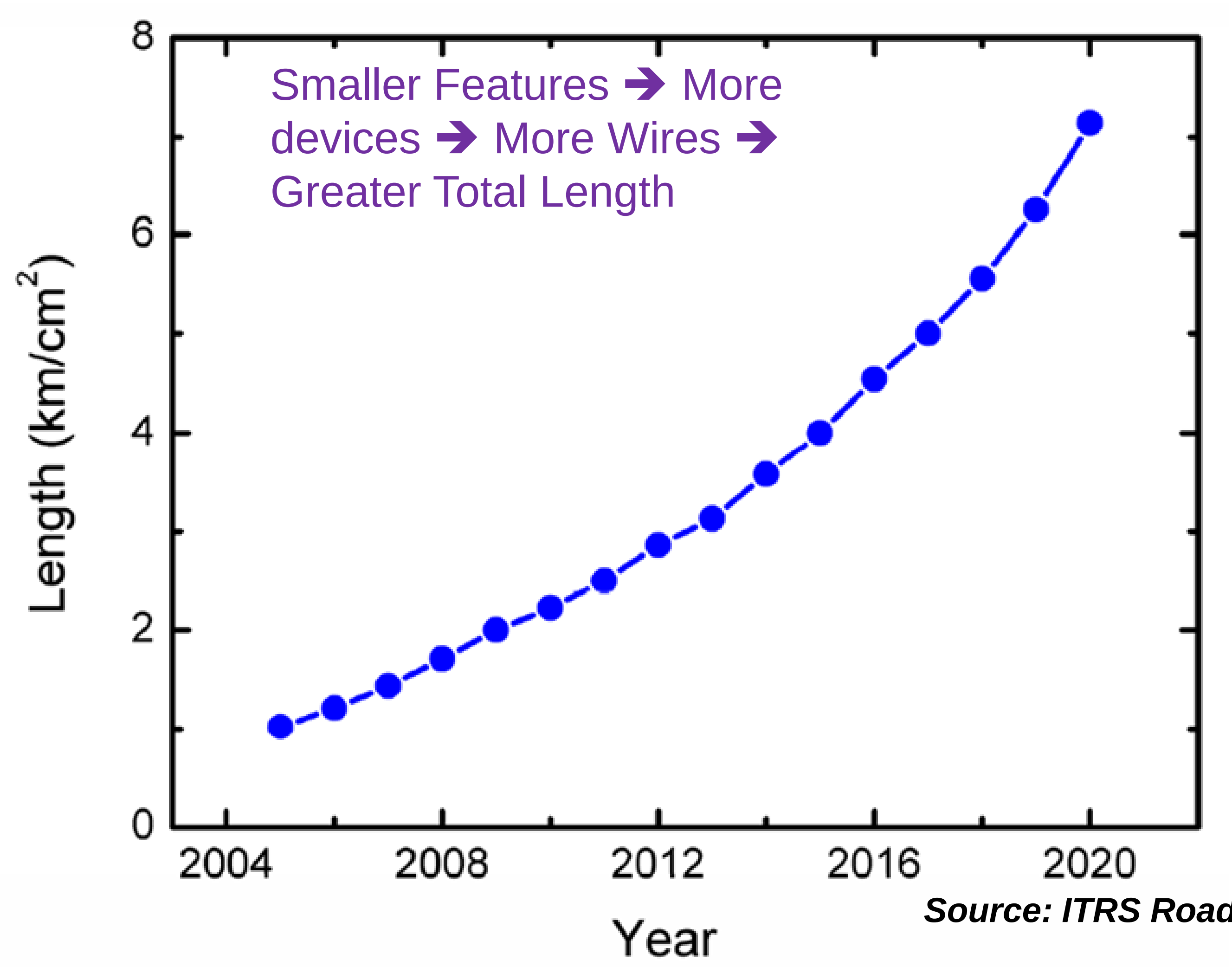
- Background & Introduction
- Electromigration: Basics, Causes, Remedies
- EM Analysis for Integrated Circuits
  - Analog dominated, small chips
  - Full-Chip EM Analysis for Large SoCs & Challenges
    - Power Grid
    - Signal Nets
- Future Directions
- References

Wire Widths Decreasing Exponentially with Time



Source: ITRS Roadmap 2005

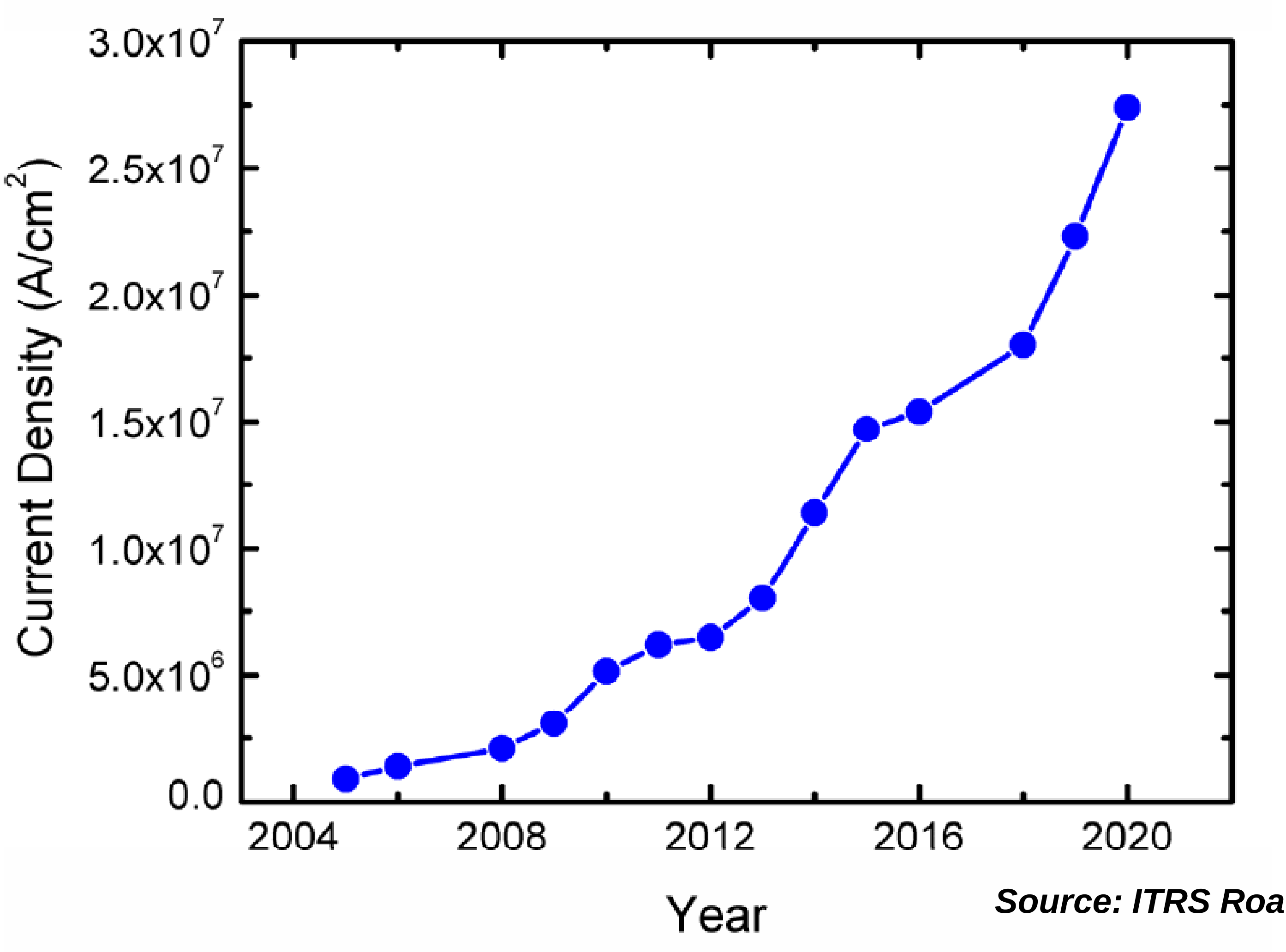
Projected TOTAL Interconnect Length Increasing Exponentially Too



Smaller Features → More devices → More Wires → Greater Total Length

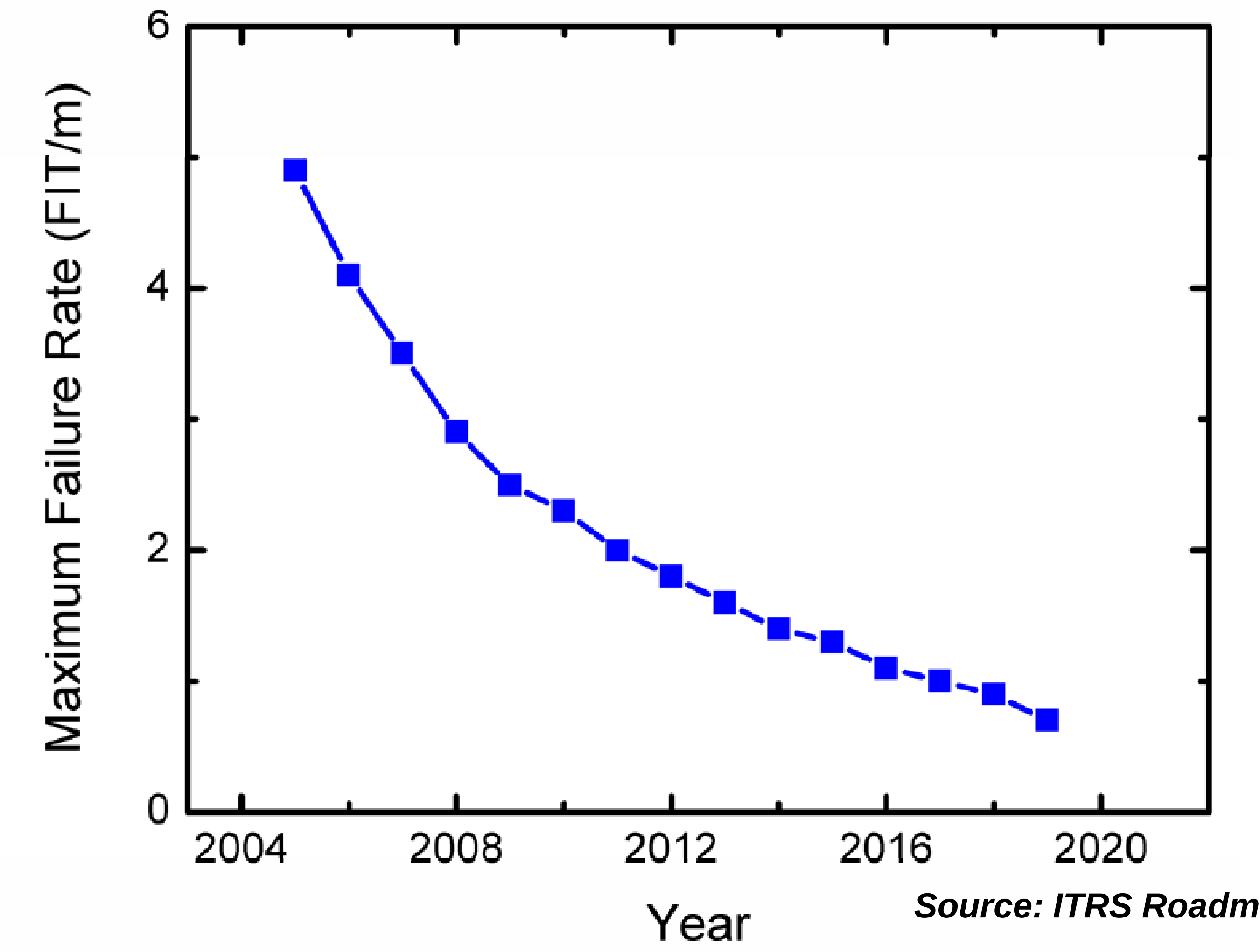
Source: ITRS Roadmap 2005

Current Density Increases Exponentially



Source: ITRS Roadmap 2005

Required Reliability Increases at an Exponential Rate



Source: ITRS Roadmap 2005

The Result…

- Wire Widths reduced to deep submicron dimensions in recent years, but their currents have not been scaled proportionally…

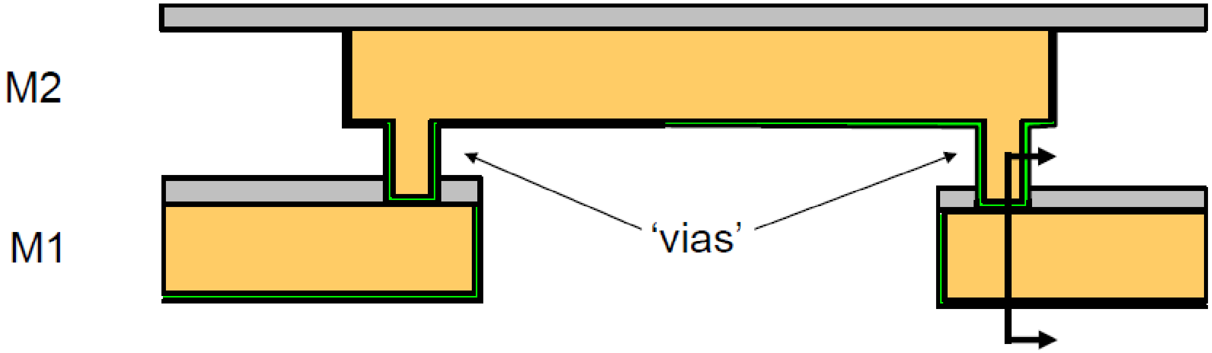
➔ VERY HIGH CURRENT DENSITIES!!!

- Temperature gradients increasingly complex and problematic
- Ever increasing susceptibility to Electromigration failures

What is Electromigration?

- EM is the gradual displacement of metal atoms in a semiconductor
  - It occurs when the current density is sufficiently high to cause the drift of metal ions in the direction of the electron flow, and is characterized by the ion flux density
  - This density depends on the magnitude of forces that tend to hold the ions in place, i.e., the nature of the conductor, crystal size, interface and grain-boundary chemistry, and the magnitude of forces that tend to dislodge them, including the current density, temperature and mechanical stresses

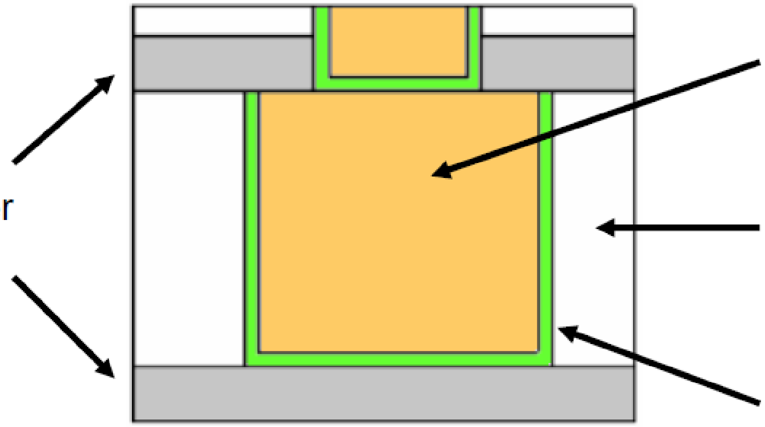
Cu Interconnect Architecture



M2

M1

'vias'



Cu

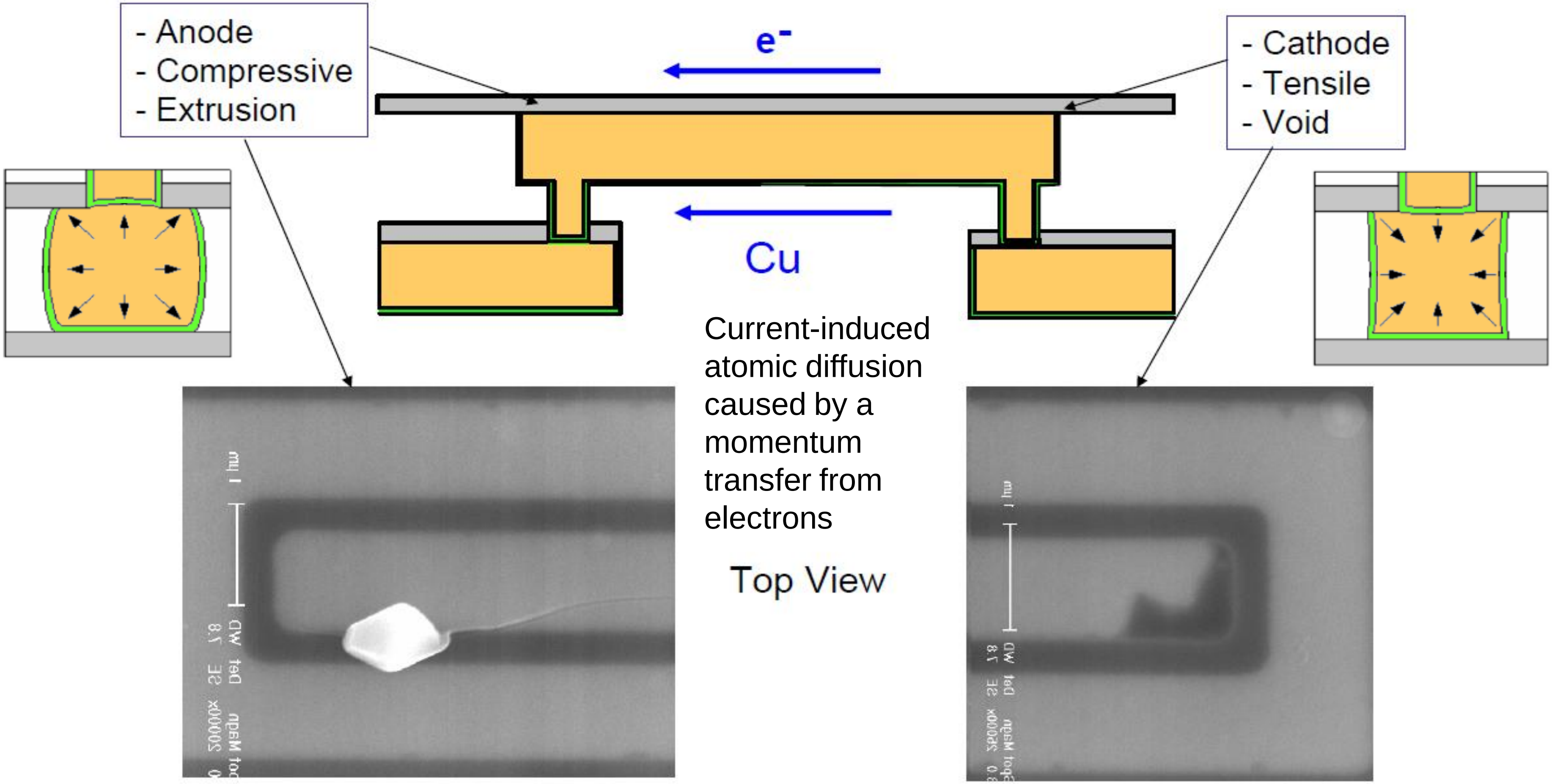
interlayer
diffusion barrier
(e.g. SiNC)

low-k dielectric
(e.g. SiCO)

diffusion barrier
(e.g. Ta)

Source: Electromigration in Integrated Circuits, Carl V. Thompson et al, Dept. of Materials Science and Engineering, MIT

Electromigration…



- Anode
- Compressive
- Extrusion

- Cathode
- Tensile
- Void

Current-induced atomic diffusion caused by a momentum transfer from electrons

Top View

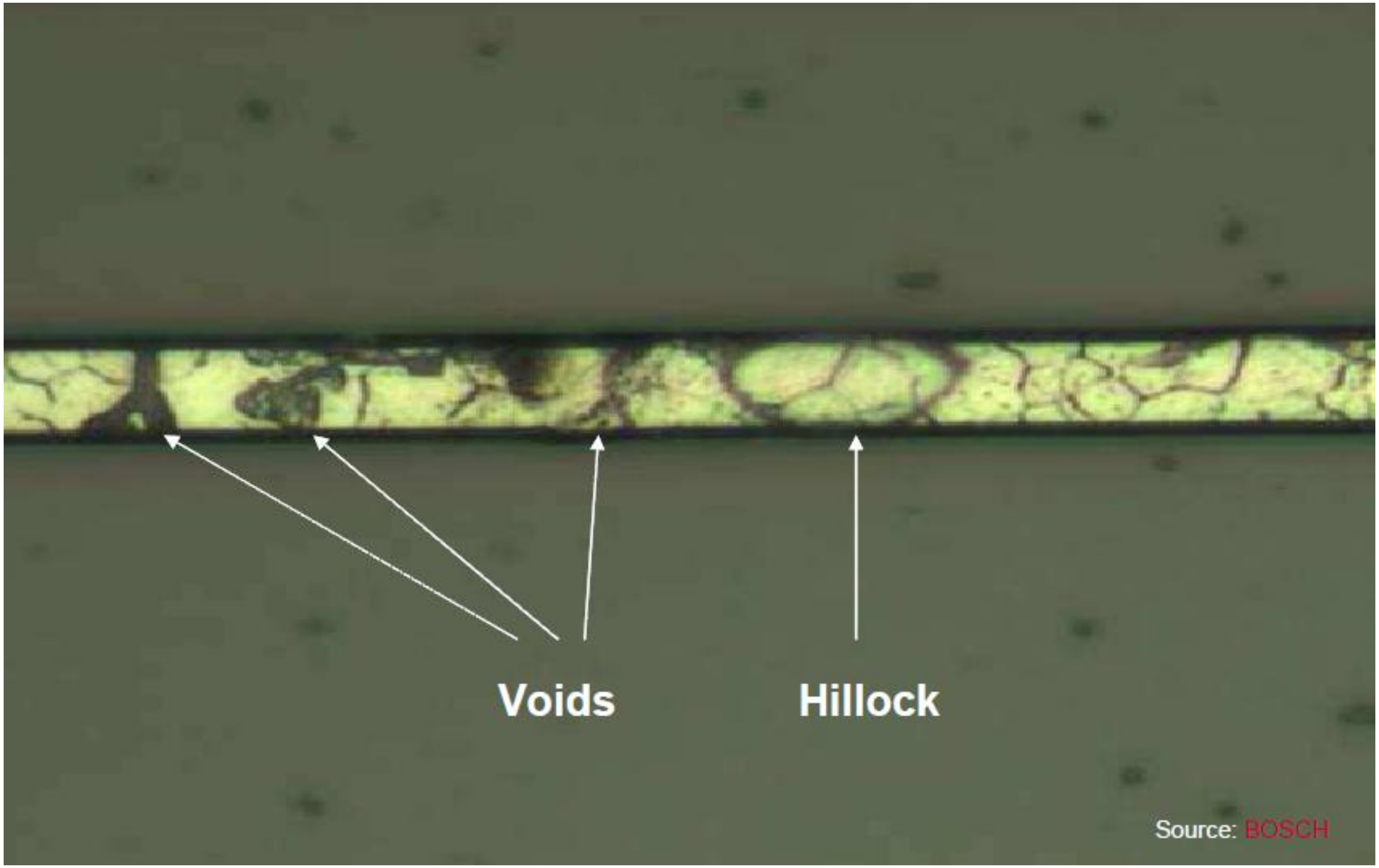
Source: Electromigration in Integrated Circuits, Carl V. Thompson et al, Dept. of Materials Science and Engineering, MIT

Electromigration…

- EM failures arise:
  - If a ***void***, created at a point where the flux of the outgoing ions exceeds the incoming flux, becomes large enough to cause an open in the metal line, or
  - A ***hillock***, leading to a short to the adjacent or overhead metal runs, is caused when the ions are piled up at a point where the incoming ion flux exceeds the outgoing flux

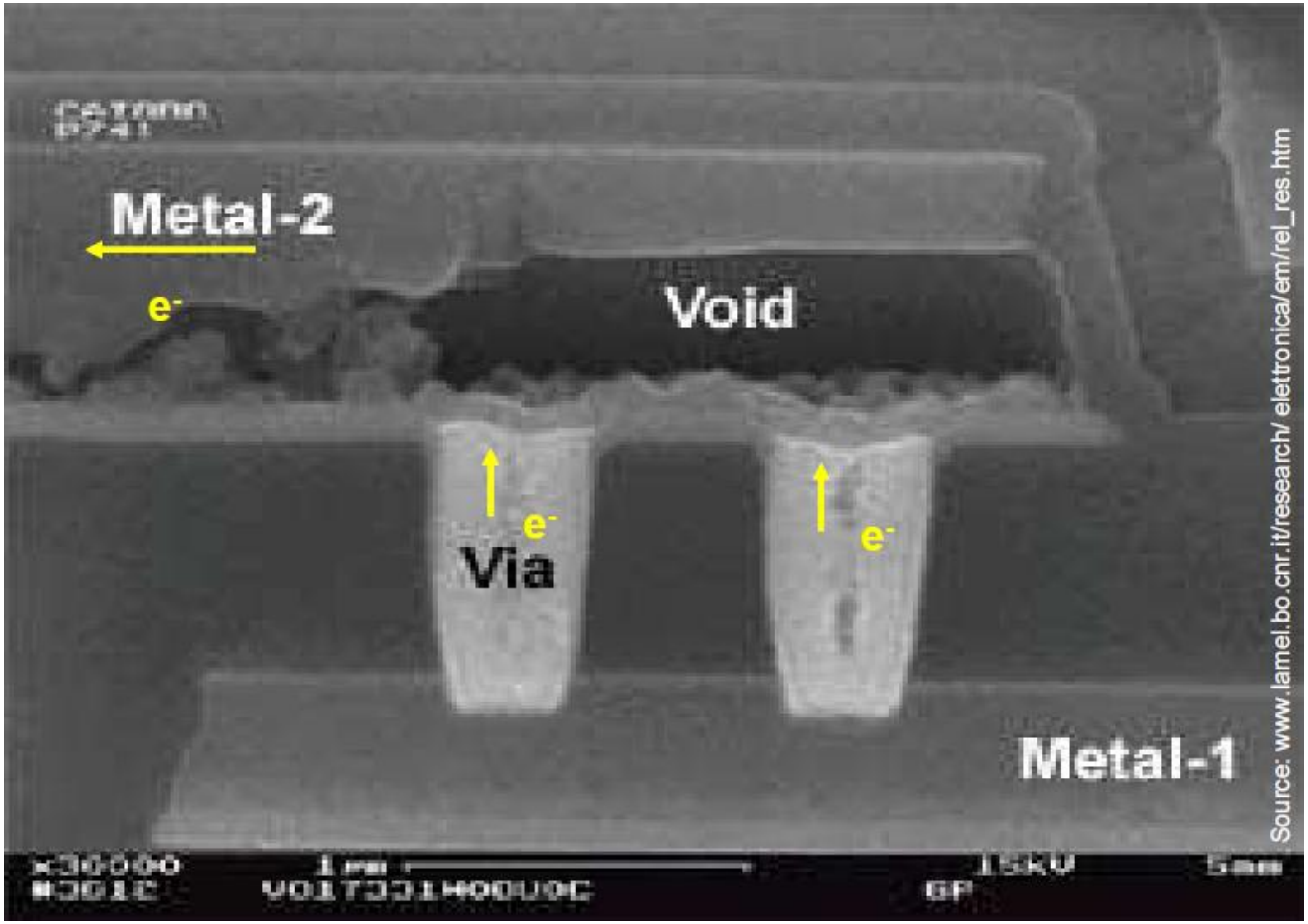
(Failures occur when there is an asymmetry in the ion flow, caused by the afore-said factors)

Voids & Hillocks



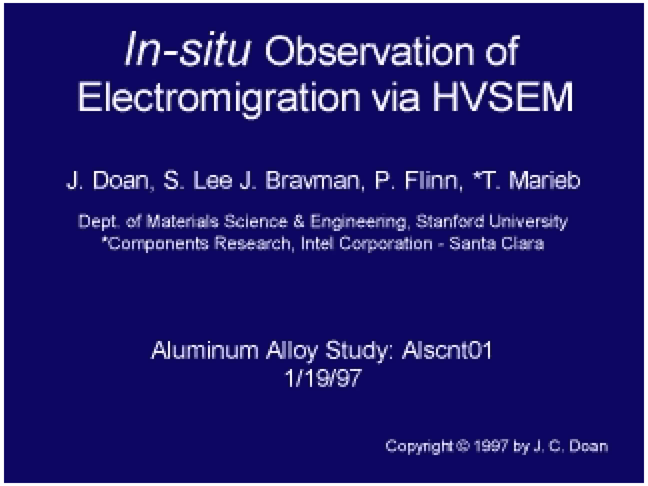
Source: Bosch (Through Cadence Whitepaper at http://www.cadence.com)

Electromigration…



Source: www.lamel.bo.cnr.it/research/ elettronica/em/rel_res.htm

Electromigration in Action: Videos



In-situ Observation of
Electromigration via HVSEM

J. Doan, S. Lee J. Bravman, P. Flinn, *T. Marieb

Dept. of Materials Science & Engineering, Stanford University
*Components Research, Intel Corporation - Santa Clara

Aluminum Alloy Study: Alscnt01
1/19/97

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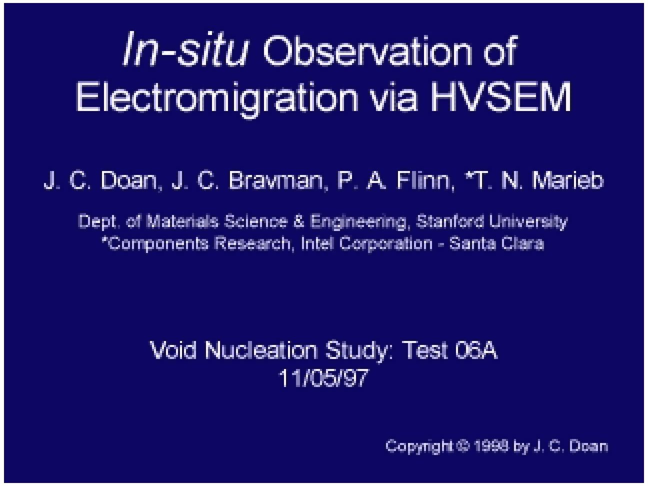

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Void Nucleation Study: Test 06A
11/05/97

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MTTF: Mean Time To Failure: Black’s Equation

$$\mathbf{t_{50} = CJ^{-n}e^{(Ea/kT)}}$$

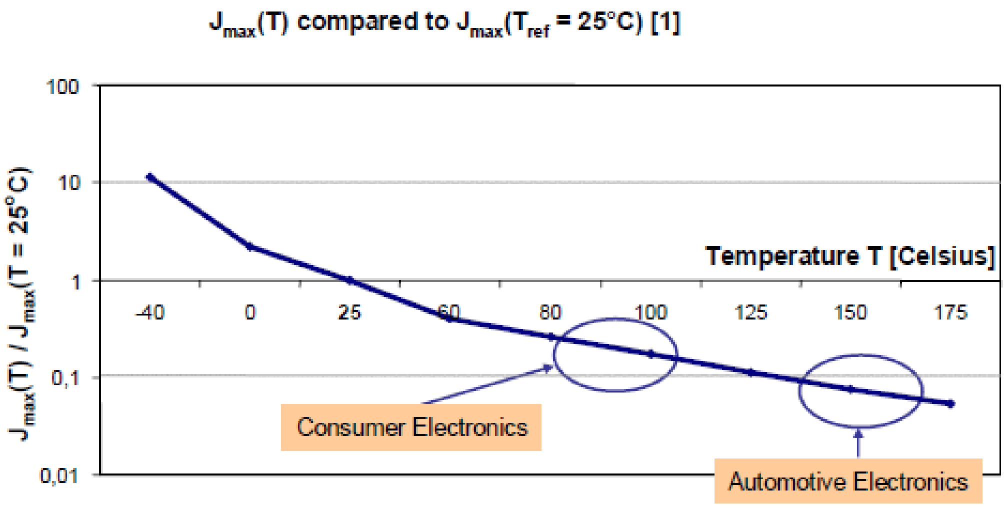
Where:

- t50 = the median lifetime of the population of metal lines subjected to electromigration;
- C = a constant based on metal line properties;
- J = the current density;
- n = integer constant from 1 to 7; many experts believe that n = 2; (many people use n, as either 2 for nucleation dominated failure or 1 for growth dominated failures)
- T = temperature in deg K;
- k = the Boltzmann constant; and
- Ea = Activation Energy (0.5 - 0.7 eV for pure Al.)

Design Constraints Effecting Electromigration

- Wire Material
  - It is known that pure copper used for Cu-metallization is more electromigration-robust than aluminum. Copper wires can withstand approximately five times more current density than aluminum wires while assuming similar reliability requirements
- Wire Temperature
  - In Black’s equation, the temperature of the conductor appears in the exponent, i.e. it strongly affects the MTTF of the interconnect. The temperature of the interconnect is mainly a result of the chip environment temperature, the **self-heating effect** of the current flow, the heat of the neighboring interconnects or transistors, and the thermal conductivity of the surrounding materials.

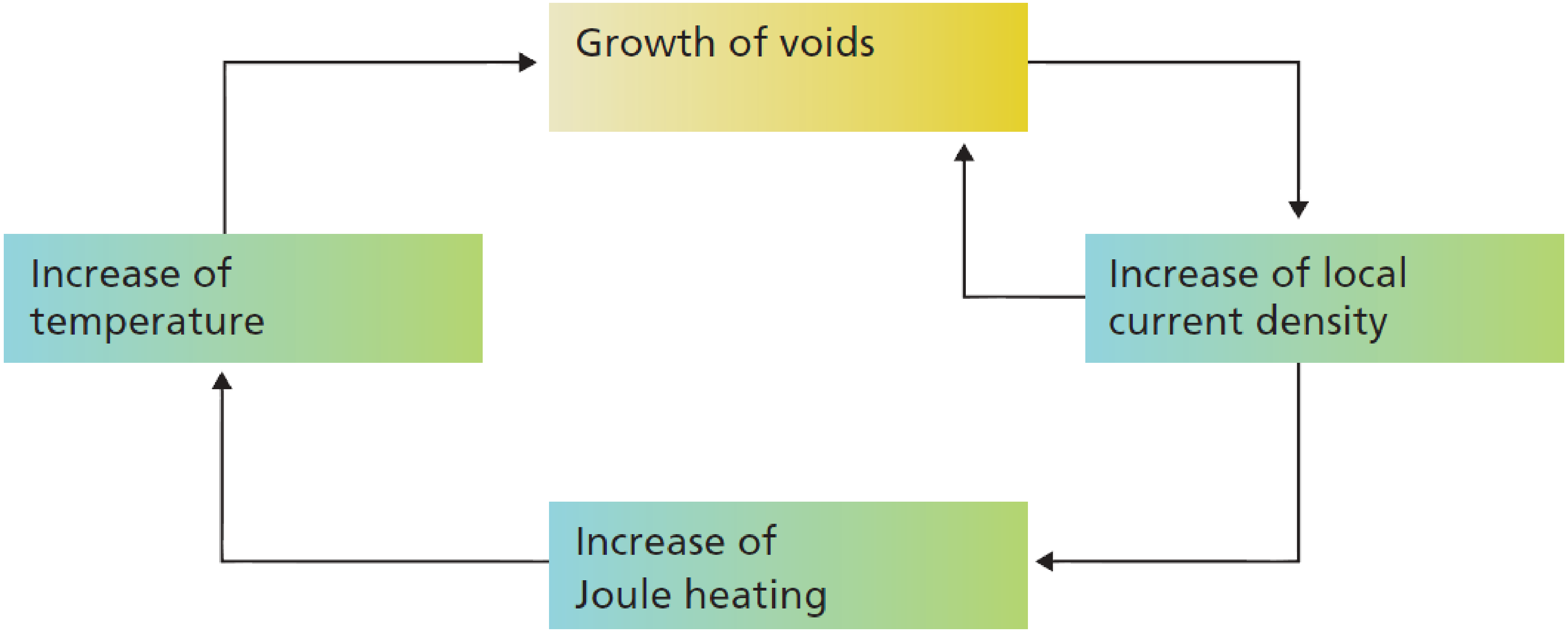
Constraints Effecting Electromigration (Contd.)



- The maximum permissible current density of an aluminum metallization, calculated at e.g. 25°C, is reduced significantly when the temperature of the interconnect rises

Source: Jens Lienig, "Introduction to Electromigration-Aware Physical Design", ISPD'06, April 9–12, 2006, San Jose, CA, USA, pp. 39-46

Wire-Self-Heating (Joule Heating)



Growth of voids

Increase of local current density

Increase of Joule heating

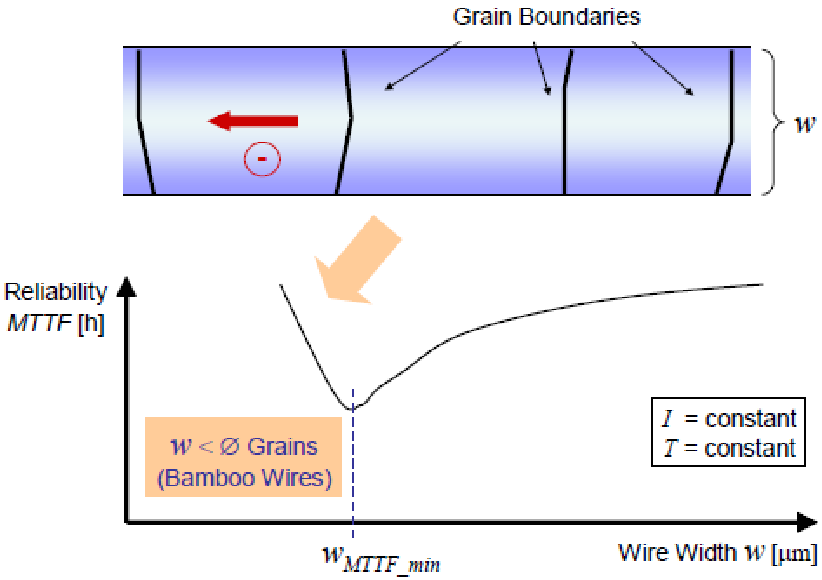
Increase of temperature

- *The cyclical relationships among temperature, current density and Joule heating. [Source- 2005 Computer Simulation Lab (Metallurgical & Materials engineering)]*

Constraints Effecting Electromigration (Contd.)

- Wire Size & Metal Slotting
  - As Black's eqn shows, apart from the temperature, it is the current density that constitutes the main parameter affecting the MTTF of a wire. Since the current density is obtained as the ratio of current *I and cross-sectional area A, and since most process* technologies assume a constant thickness of the printed interconnects, it is the wire width that exerts a direct influence on current density: The wider the wire, the smaller the current density and the greater the resistance to electromigration
  - However, there is an exception to this accepted wisdom: If you reduce wire width to below the average grain size of the wire material, the resistance to electromigration increases, despite an increase in current density. This apparent contradiction is caused by the position of the grain boundaries, which in such narrow wires as in a bamboo structure lie perpendicular to the width of the whole wire

Constraints Effecting Electromigration (Contd.)

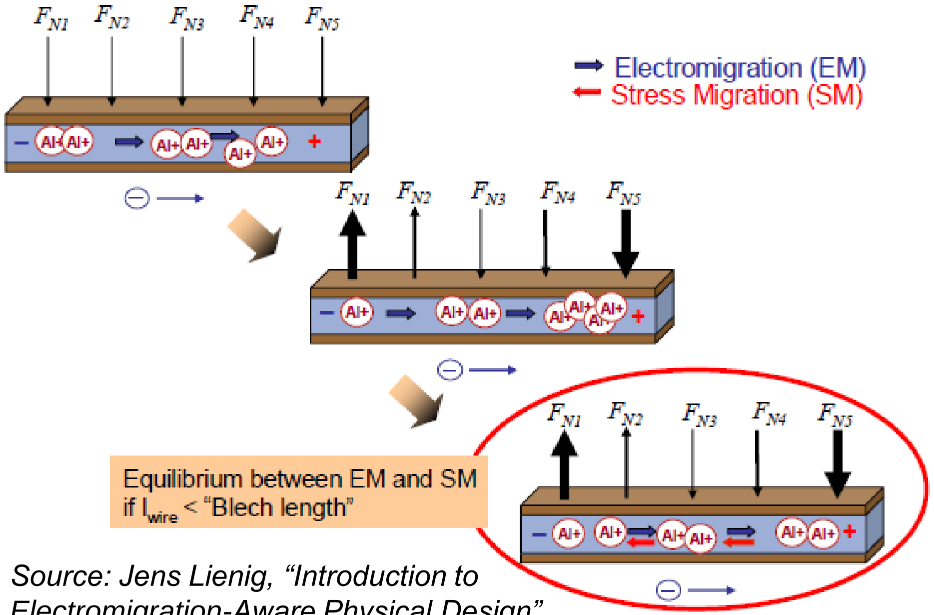


Source: Jens Lienig, "Introduction to Electromigration-Aware Physical Design", ISPD'06, April 9–12, 2006, San Jose, CA, USA, pp. 39-46

- Reduced wire width below the average grain size increases the reliability of the wire with regard to electromigration. So-called bamboo wires are characterized by grain boundaries which lie perpendicular to the direction of the electron wind and thus permit only limited grain boundary diffusion

Constraints Effecting Electromigration (Contd.)

- Wire Length
  - There is also a lower limit for the length of the interconnect that will allow electromigration to occur. It is known as “***Blech-length***”, and any wire that has a length below this limit (typically in the order of 10-100 µm) will not fail by electromigration
  - Here, a mechanical stress buildup causes a reversed migration process which reduces or even compensates the effective material flow towards the anode



Source: Jens Lienig, “Introduction to Electromigration-Aware Physical Design”, ISPD’06, April 9–12, 2006, San Jose, CA, USA, pp. 39-46

Specifically, a conductor line is not susceptible to electromigration if the product of the wire’s current density J and the wire length l is smaller than a process technology dependent threshold value (J·l)threshold

Constraints Effecting Electromigration (Contd.)

- Via arrangements & Corner-bends
  - Particular attention must be paid to vias and contact holes, because generally the ampacity of a (tungsten) via is less than that of a metal wire of the same width. Hence multiple vias are often used, whereby the geometry of the via array is very significant: Multiple vias must be organized such that the resulting current flow is distributed as evenly as possible through all the vias
- Terminal Connections
  - Analog terminals (pins) are distinguished by a great variety of shapes and sizes. When connecting such a terminal to a wire, designers must bear in mind that different connection positions of a wire to this terminal can cause different current loads within the terminal structure. For this reason, a current density verification should include not only the interconnects, but also all terminal structures.

Thus, Common “Cures” for EM Issues

- Wire widening to reduce current density
  - Bigger power grids for power nets (putting power grids on thicker layers) & Wire-widening for signal nets
  - What are your decisions based on? Relying only on global design rules may result in overdesign
  - Besides, need to be aware of “dishing” effect (CMP)
- Providing redundant vias
- Designing the circuit to run at lower voltage levels
- Controlling temperature by using a thermal-aware IC design methodology
- Good power management techniques will generally reduce EM, lowering power dissipation & controlling voltage drop would help
- DFM techniques that reduce variability

Full-Chip EM Analysis

- Especially at advanced nodes, full-chip reliability analysis is becoming increasingly critical (narrower interconnect structures, higher-frequency designs which increases the overall current density and therefore the risk of electromigration and Joule heating failures in designs)
  - Preventive measures are required during the design process in order to reduce the risk of chip failures
- Traditionally, designers are given simple wire current density limits to which they must adhere - these limits are based on “worst case“ estimates of the current density that is expected under use conditions, usually maximum temperature → Over-restrictive
  - Sample this: if the industry-typical maximum current density of 2x(10)5 A / cm2 were passed through most conductors, a chip dissipating **kilowatts** would be required!!!

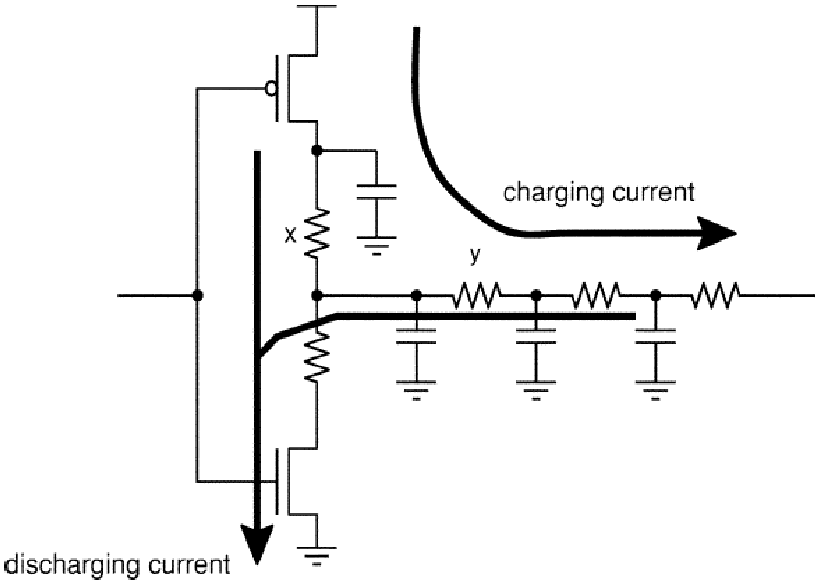
Full-Chip EM Analysis (Contd.)

- To avoid overdesign and to permit engineering compromises between design size and lifetime, reliability budgeting is being done
  - It estimates the probability that the chip will operate properly over its projected lifetime
  - The estimate are performed using circuit analysis to obtain realistic estimates of actual currents flowing in the wires, the application of advanced electromigration models to wire segments, such as Black’s equation, and statistical analysis over the wires in the design

EM Analysis (Contd.)

- Electromigration analysis is separated into two steps:
  - The first step checks for violations of the ***current density*** limits, and
  - The second step assesses the ***mean-time-to-failure (MTTF)*** for all wire segments
- The analysis is based on parasitic RC networks extracted from layout and estimated or calculated current distribution in each segment of the interconnect structures
  - The extracted RC network must include line width and layer information to enable electromigration analysis

Unidirectional & Bidirectional Currents

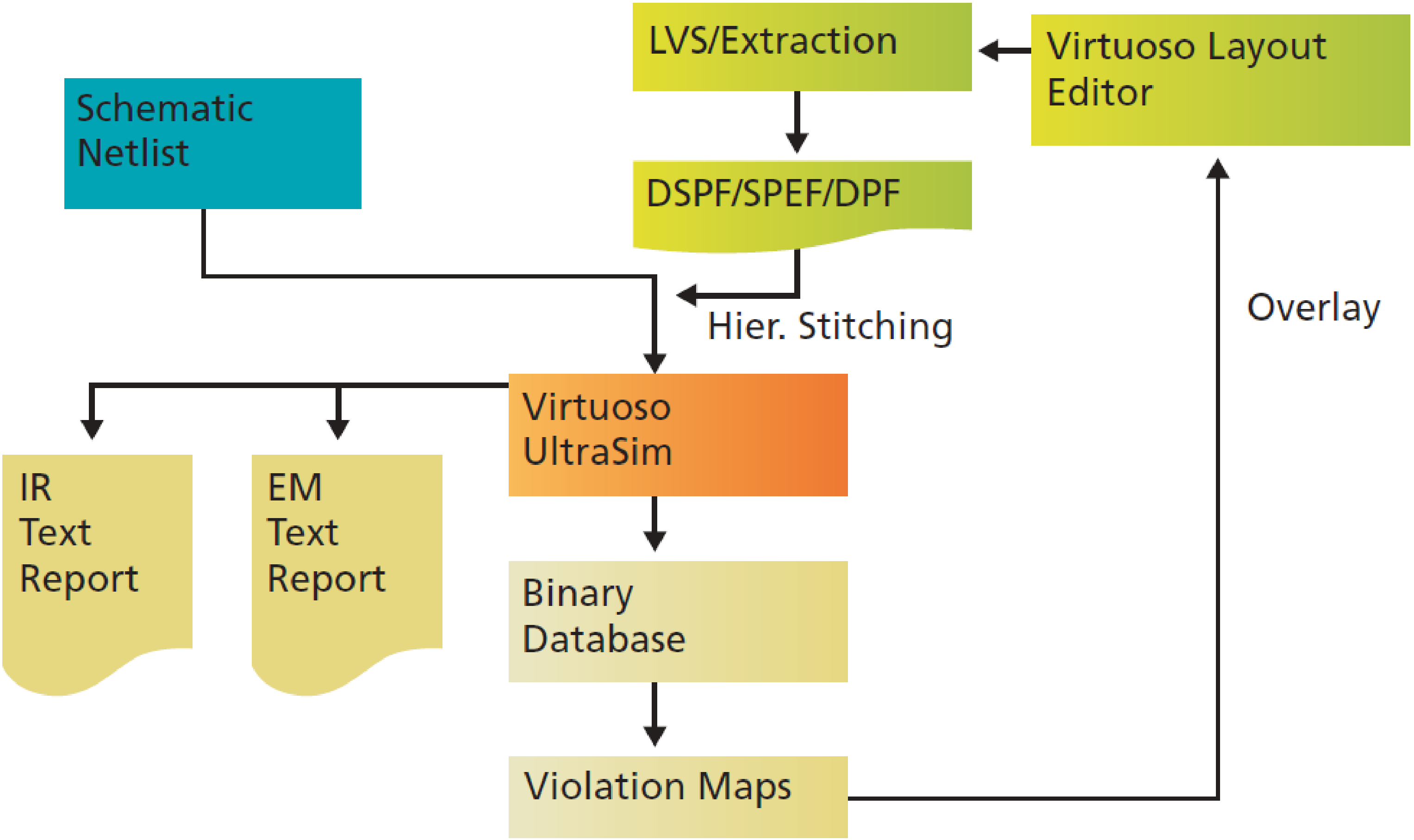


- **Unidirectional** current through segment "x" for a rising and falling transition is shown. In this case, the Idc current value is nonzero and the likely failure mechanism will be due to dc current stress
- **Bidirectional** current through segment "y" is shown. For this wire segment, Idc is close to zero and the likely failure mechanism is due to Joule heating. In this case, the Irms and Ipeak currents will determine the lifetime of the segment
- A wire segment may have both significant Idc and Irms/ Ipeak under different driver configurations. EM analysis, thus requires the calculation of all three currents

EM Analysis (Contd.)

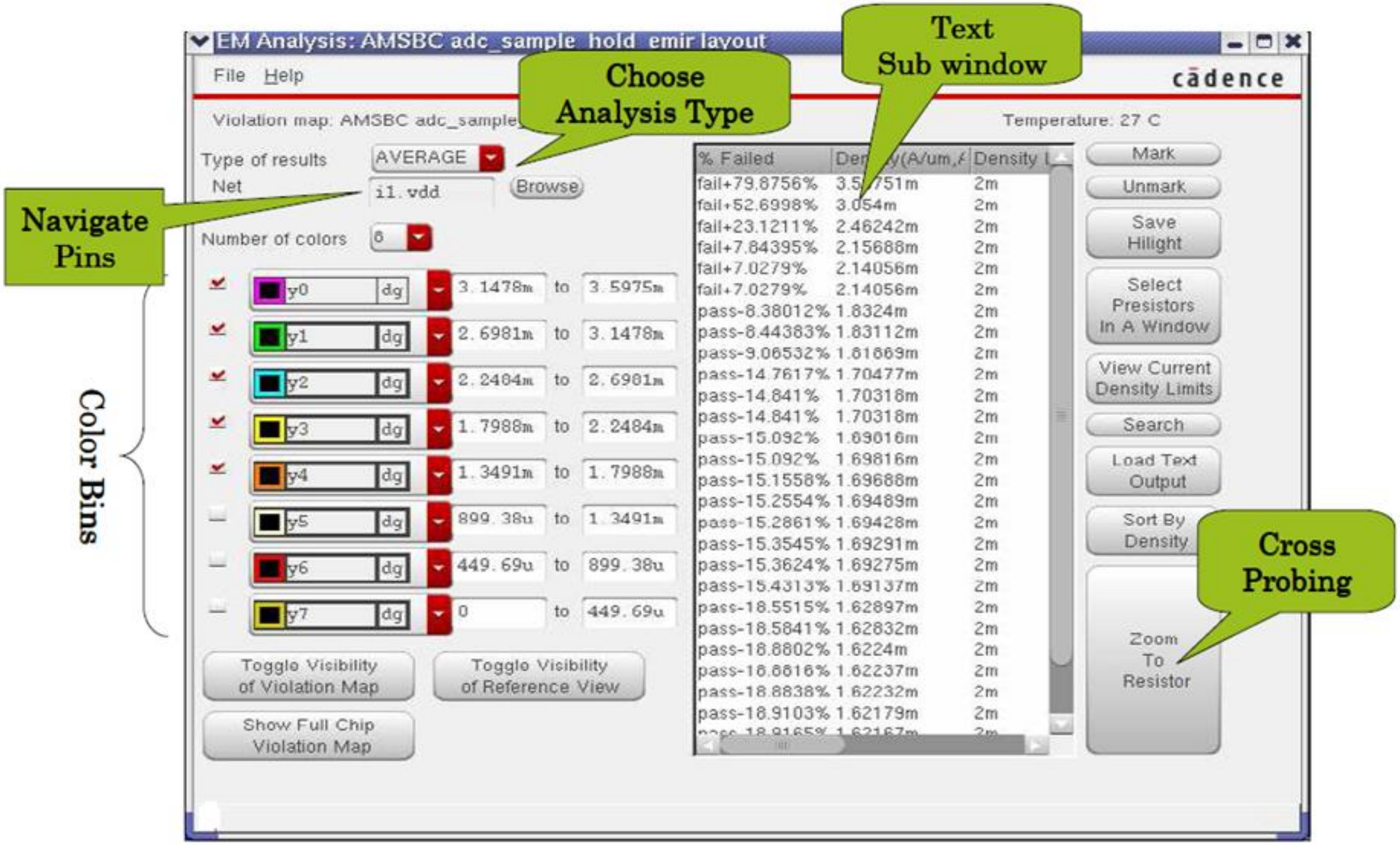
- Typically, electromigration has involved the process of time-domain simulation of drivers and interconnect to obtain average, root mean square (rms), and peak current values for each wire segment
  - Idc would suffice for Power nets
- A dynamic approach to circuit-level electromigration analysis uses simulation of the interconnect with a Spice-level simulation tool to obtain time-varying current waveforms for each interconnect segment. Based on these current waveforms, average, rms, and peak current values can be easily calculated

Typical EM Analysis Flow



(Source: Cadence Design Systems, http://www.cadence.com)

EM Report



Violation map: AMSBC adc_sample

Temperature: 27 C

Type of results: AVERAGE

Net: i1.vdd

Number of colors: 6

☑	y0 dg	3.1478m	to	3.5975m
☑	y1 dg	2.6981m	to	3.1478m
☑	y2 dg	2.2484m	to	2.6981m
☑	y3 dg	1.7988m	to	2.2484m
☑	y4 dg	1.3491m	to	1.7988m
☐	y5 dg	899.38u	to	1.3491m
☐	y6 dg	449.69u	to	899.38u
☐	y7 dg	0	to	449.69u

% Failed	Den y(A/um,	Density L
fail+79.8756%	3.5 751m	2m
fail+52.6998%	3.054m	2m
fail+23.1211%	2.46242m	2m
fail+7.84395%	2.15688m	2m
fail+7.0279%	2.14056m	2m
fail+7.0279%	2.14056m	2m
pass-8.38012%	1.8324m	2m
pass-8.44383%	1.83112m	2m
pass-9.06532%	1.81869m	2m
pass-14.7617%	1.70477m	2m
pass-14.841%	1.70318m	2m
pass-14.841%	1.70318m	2m
pass-15.092%	1.69016m	2m
pass-15.092%	1.69816m	2m
pass-15.1558%	1.69688m	2m
pass-15.2554%	1.69489m	2m
pass-15.2861%	1.69428m	2m
pass-15.3545%	1.69291m	2m
pass-15.3624%	1.69275m	2m
pass-15.4313%	1.69137m	2m
pass-18.5515%	1.62897m	2m
pass-18.5841%	1.62832m	2m
pass-18.8802%	1.6224m	2m
pass-18.8816%	1.62237m	2m
pass-18.8838%	1.62232m	2m
pass-18.9103%	1.62179m	2m
pass-18.9165%	1.62167m	2m

Text Sub window

Choose Analysis Type

Navigate Pins

Color Bins

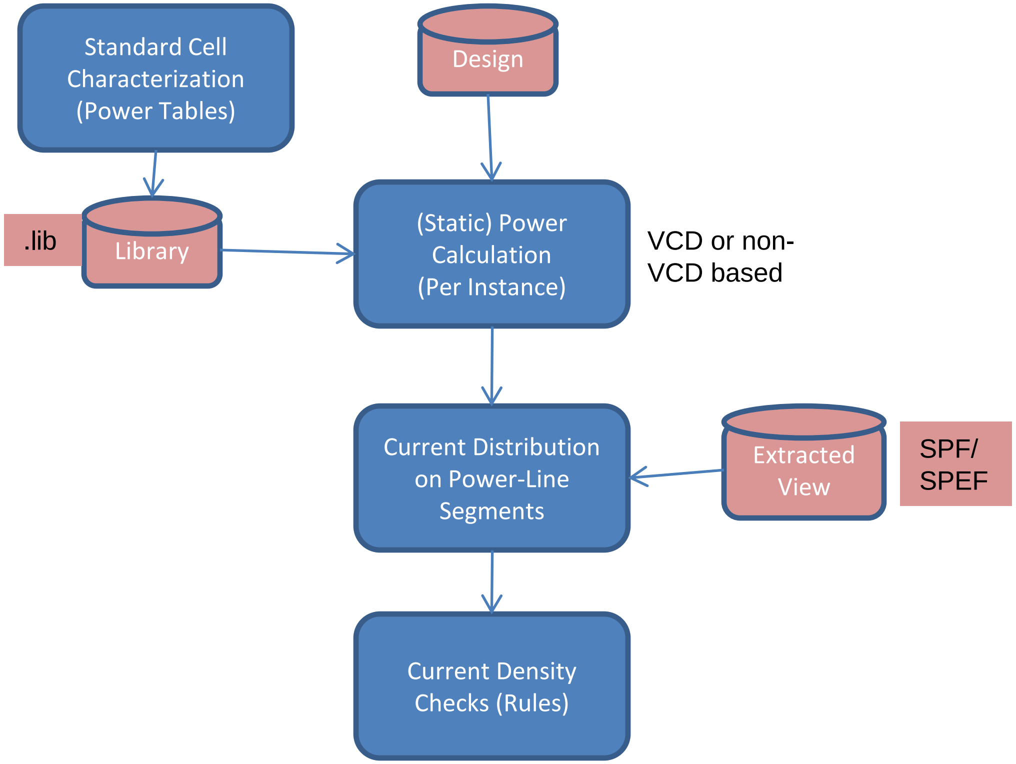
Cross Probing

(Source: CDNLive 2007, www.cadence.com)

Full Chip EM Analysis Challenges

- As we saw, typically, EM involves the process of time-domain simulation of drivers and interconnect - this approach cannot be applied to large problem sizes where hundreds of thousands of nets must be analyzed, each consisting of many thousands of RC elements
- Various "filtering" mechanisms have been proposed to identify and filter EM "immortal" nets (eg. The jL filter – Blech Length)
  - Even the number of nets post filtering multiplied by number of elements on each net is very high for a Spice level simulation
- Various "Static" Approaches have been proposed for determination of the current and current densities
  - For Power-Grids
    - Relatively easier due to primarily DC current behavior etc
  - For Signal Nets
    - More complex given the complex bi-directional current behavior, complex interconnect topologies & volume

(Static) Full Chip Power EM Flow



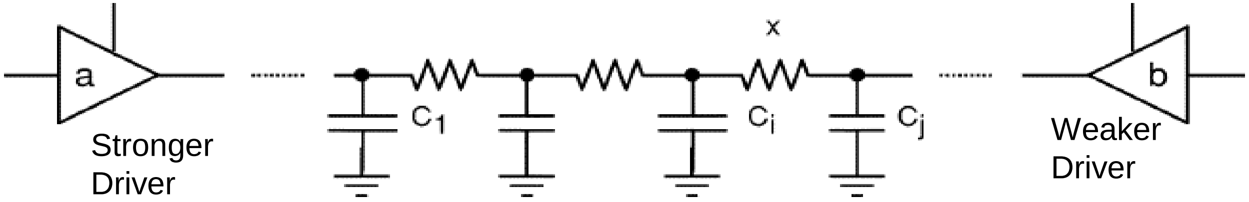
- The power grid of a chip is operated primarily in a pulsed DC sense with respect to electromigration analysis: electromigration driving force is determined by the average current density
  - Calculates the average current drawn by each transistor connected to the power grid
  - One at a time, each power grid is modeled by voltage sources at the pins providing power to the chip and the transistor tap currents at the device connection points
  - The large linear system is then solved to determine the precise current flowing through every power-line segment and via in the chip

Signal EM Analysis: Complexities

- Huge number of signal nets in a complex chip
  - Each signal net can easily consist of tens of thousands of R/C elements and the number of nets that need to be analyzed can easily reach hundreds of thousands for a large microprocessors
- RMS Currents & Joule Heating
  - In addition to the electromigration lifetime based on the average current, the RMS current also needs to be calculated
  - Joule heating depends on RMS current and it must be realized that RMS current always exceeds average current for any duty cycle less than one
  - Joule heating produces temperature gradients that can cause failure due to temperature gradient induced flux divergences
  - RMS current is treated as an absolute “speed limit” and exceeding the limiting value is not permitted

Signal EM Analysis: Complexities (Contd.)

- Complex bidirectional Current Flows
  - The analysis is further complicated by the fact that each signal net often has multiple drivers that can switch in different ways



  - In order to obtain the maximum average current value for ‘x” , the net is driven high through “a” , while driver “b” is in tristate mode and then the net is driven low with driver “b”, while driver “a” is in tristate mode. During the rising transition, capacitor Cj is charged through “x”, while in the falling transition, capacitors C1 through Ci are discharged through “x”. The same charge transfer would be obtained if drivers “a” and “b” were interchanged

Signal EM Analysis: Complexities (Contd.)

- On the other hand, the worst rms current may occur when the net is switched both high and low with either driver “a” or with driver “b”. Since driver “a” is the stronger driver, it will result in a faster transition which increases the Irms/ Ipeak current in “x”. However, switching the net from driver “a” charges and discharges capacitor Cj through “x”, while switching the net from driver “b” charges and discharges capacitors C1 through Ci . Depending on the relative size of the drivers and capacitors, it is likely that if “x” is positioned near the end of the line (near driver “b”), driver “b” will result in the maximum Irms/ Ipeak current, while driver ‘a” may result in the worst Irms/ Ipeak current if is positioned closer to the start of the line (near driver “a”). Therefore, the worst case driver transition depends in a nontrivial way on the driver strengths and the interconnect topology
- In order to determine the worst case driver transition, a dynamic simulation-based approach must simulate all possible rising and falling driver transition combinations (called *switching scenarios) for* an interconnect and therefore incurs a high run time cost. It also requires the user to perform the laborious and error-prone task of writing simulation vectors

Sample EM “Rules”

- Short length rules : Any wire segment below certain length (Blech Length) is treated as EM-proof
- Long length rules
  - Current density limit a factor of width of the wire segment and temperature
  - Current density limit on a metal is a factor of number of vias connected to the segment and also current direction
  - Peak, rms, avg current rules
  - AC limits are generally high then dc due to recovery factor
- Examples
  - Short Length Rules

$$I_{MAX}(5 \le L \le 10) \propto \frac{W * S}{L}$$

$$I_{MAX}(L < 5) \propto \frac{W * S}{5}$$

where, W ➔ Segment Width;
L ➔ Segment Length;
S ➔ De-rating Factor;
T ➔ Simulation Temperature

Sample EM “Rules” (Contd.)

- Long Length Rules

$$I_{MAX}(2 \geq W \geq 20) \propto W * S$$

$$I_{MAX}(2 < W < 20) \propto W * \sqrt{W} * S$$

$$S \propto e^{1/T}$$

$$T > 80C$$

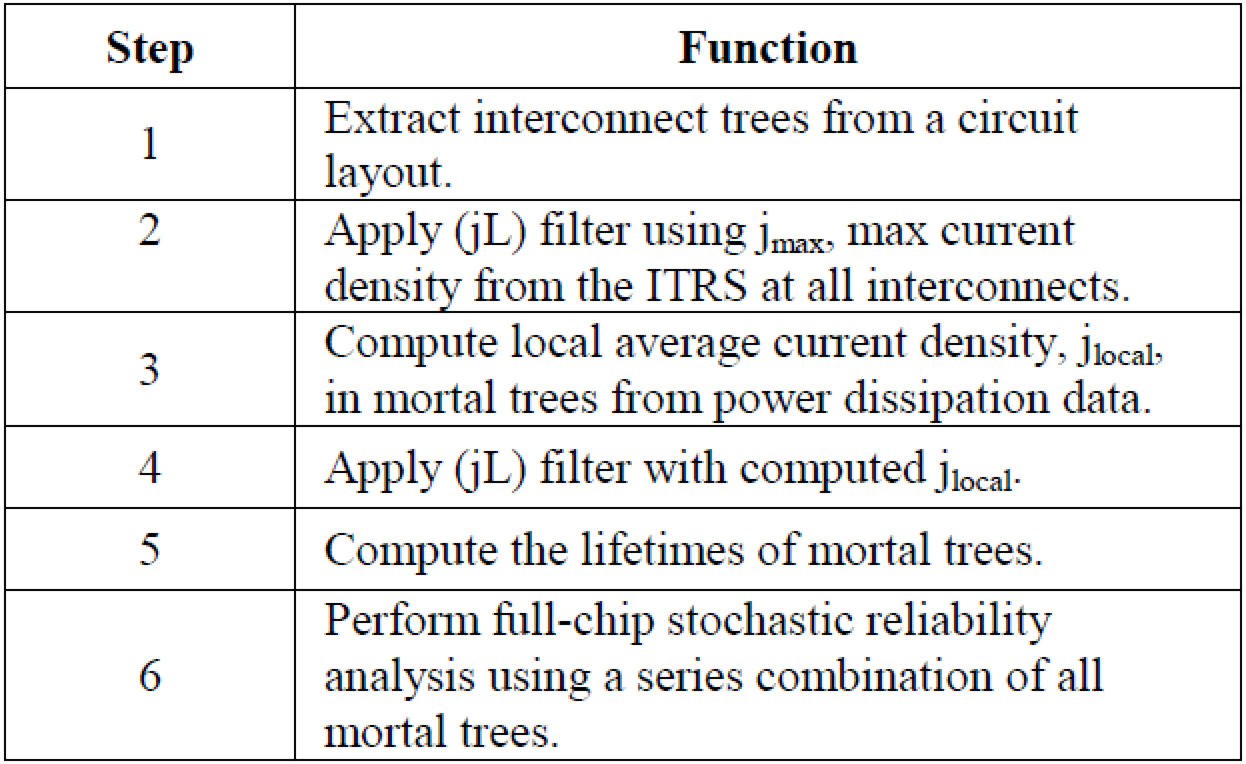
- While most interconnect segments exhibit AC current behavior, almost every signal interconnect lines on a chip includes interconnect segments that exhibit DC current behavior. Therefore signal wires must be checked for **both average and RMS current** density violations:
  - Average current density checks detect those wire segments with high levels of unidirectional current that impact the electromigration resistivity
  - RMS current density checks detect those wire segments that suffer from Joule heating induced failure mechanisms. In addition, peak current density limits must be validated to avoid fusing of vias or contacts

Full-Chip Signal EM Analysis

- Various approaches have been proposed, do not seem to have a good production solution from EDA companies
  - Primarily because of the complexities described earlier and not enough compelling push by the semiconductor companies
    - Many home-grown work-arounds / utilities exist though

- Ensuing slides give a brief overview of some of these approaches

Typical Full-Chip Signal EM Analysis Flow



Step	Function
1	Extract interconnect trees from a circuit layout.
2	Apply (jL) filter using j_{max}, max current density from the ITRS at all interconnects.
3	Compute local average current density, j_{local}, in mortal trees from power dissipation data.
4	Apply (jL) filter with computed j_{local}.
5	Compute the lifetimes of mortal trees.
6	Perform full-chip stochastic reliability analysis using a series combination of all mortal trees.

Cumulative Probability of Failure

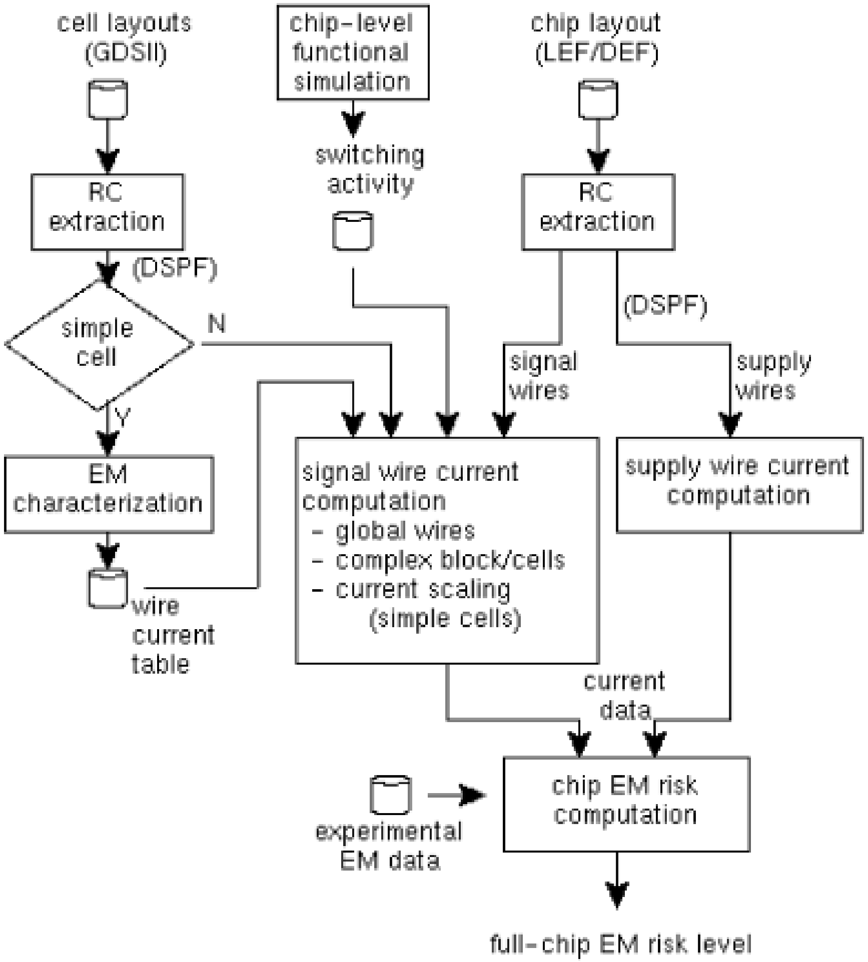
- The cumulative probability of failure for a projected lifetime Pfi(t), is approximated using multiple methodologies/ stochastic models
- One of the more widely used distribution is extreme lognormal and a sample cumulative probability function is given as:

$$P_{fi}(t) = \frac{\sigma}{\sqrt{2\pi}\ln\left(t_{50}/t\right)} \exp - \left[\frac{\ln\left(t_{50}/t\right)}{\sqrt{2}\sigma} \right]^2$$

Full-Chip Signal EM: Blauu et al

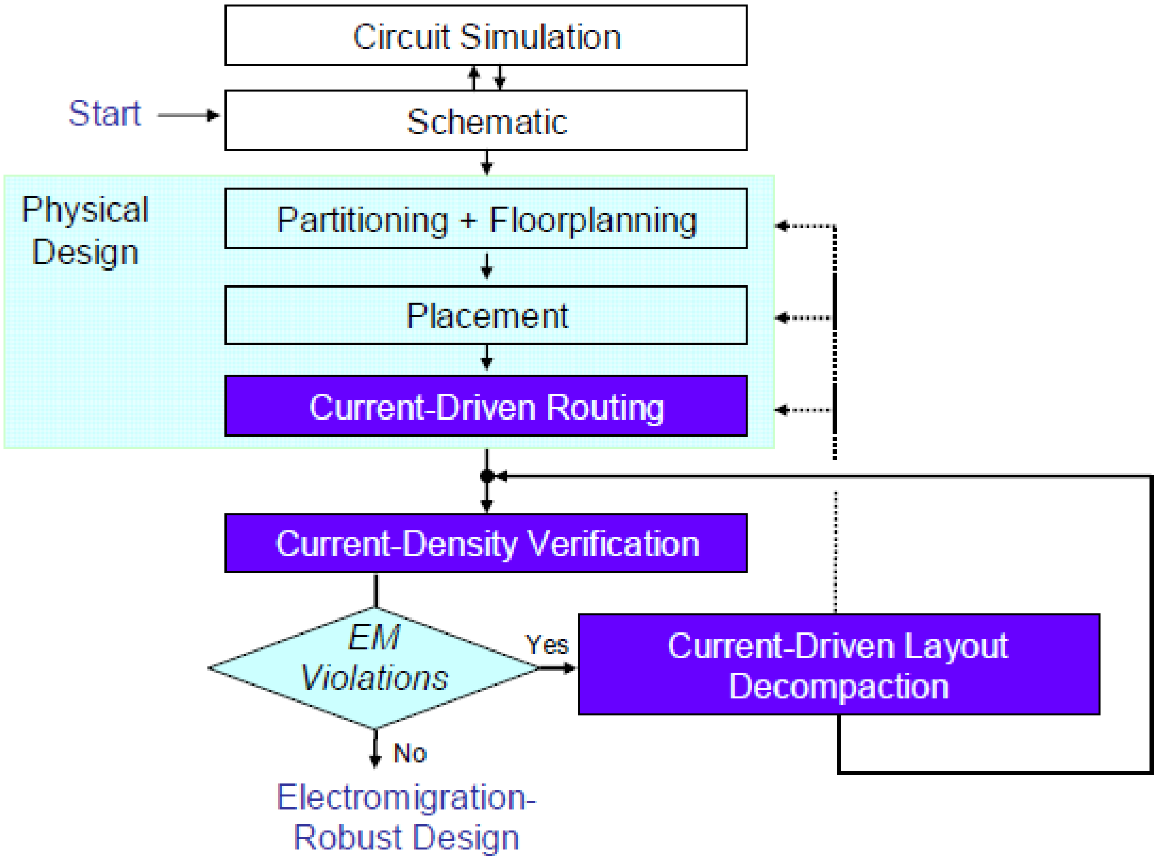
- The authors propose a static electromigration analysis approach
  - They show that the charge transfer through wire segments of a net can be calculated directly by **<u>solving a system of linear equations</u>**, derived from the nodal formulation of the circuit, thereby eliminating the need for time domain simulation
  - Also, they prove that the charge transfer through a wire segment is independent of the shape of the driver current waveform
  - From the charge transfer through each wire segment, the average current is obtained directly, as well as approximate rms and peak currents
  - The authors account for the different possible switching scenarios that give rise to unidirectional or bidirectional current by separating the charge transfer from the rising and falling transitions and also propose approaches for modeling multiple simultaneous switching drivers

Full-Chip Signal EM: Panda et al



- Characterization of standard cells, off-the-shelf components, and macros to exploit repetition for drastically cutting down the simulation effort
  - Pre-characterization of current on signal and power wires inside simple cells
  - Computing current on signal and power wires inside complex cells and custom macros by analyzing individual instances
- Identification of unidirectional and bi-directional current elements, and
  - computing current on global signal wires
  - computing current on global power wires

Looking Forward: EM-Aware Design Flow



Current Driven Routing & Layout Decompaction

- Current-driven routing ensures that the widths of all automatically routed interconnect structures are laid out correctly to fulfill all predefined electromigration and ESD reliability requirements
- Current-driven layout decompaction performs a post-route adjustment of layout segments with current-density violations and inhomogeneous current flows, respectively. Current-driven decompaction has been shown to be an effective point tool when addressing current-density-related violations without invoking a repetition of the entire place and route cycle.

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